**THAT WHICH IS CLAIMED IS:**

1. A detector for detecting timing in a digital data flow (BK) with a bit-time equal to T and with a coding which provides, at the beginning of the bit-time T, for no transition or for a transition of a first or a transition of a second type and, in the middle of the bit-time T, for no transition or for a transition of the first type characterized in that it comprises first circuit means (2) for generating four local timing signals (Q1-Q4) which have periods substantially equal to the bit-time and are out of phase with one another by 1/4 period, and second circuit means (3) for sampling the four local timing signals (Q1-Q4) upon each transition of the first type in the data flow and for determining, on the basis of the sampled states of the four local timing signals (Q1-Q4), whether a pair of reference signals (Q1-Q3) which are out of phase by one half period, of the four local timing signals (Q1-Q4), are advanced or delayed relative to the timing of the data flow, and consequently controlling the first circuit means in a manner such as to delay or to advance the four local timing signals (Q1-Q4).

2. A timing detector according to Claim 1, in which the coding is a CMI (coded mark inversion) coding.

3. A timing detector according to Claim 2, characterized in that the second circuit means (3) comprise circuit means (100; FF1-FF4) for sampling the four local timing signals (Q1-Q4) upon each transition of the first type in the data flow (BK), and circuit means (101; 4) which decode the sampled states of the

four local timing signals (Q1-Q4) and which control the first circuit means (2).

4. A detector according to Claim 3, characterized in that the sampling circuit means comprise four bistable elements (FF1-FF4) of which each is associated with a respective signal (Q1-Q4) of the four local timing signals and all are clocked by the transitions of the first type in the data flow (BK), and the decoding circuit means comprise a combinational circuit (4) which receives the outputs of the bistable elements (FF1-FF4) and which, on the basis of the states of the said outputs, determines whether the said pair of reference signals (Q1, Q3) are advanced or delayed relative to the timing of the data flow (BK) and consequently controls the first circuit means (2).

5. A timing detector according to Claim 4, characterized in that the bistable elements are D-type flip-flops and the combinational circuit (4) comprises an AND-OR-INVERT gate which receives the outputs of the flip-flips (FF1-FF4) as inputs.

6. A timing detector according to Claim 5, characterized in that the AND-OR-INVERT gate receives as inputs a pair of sampled signals (Q1', Q3') corresponding to the pair of reference signals (Q1, Q3), and a second pair of sampled signals (Q2N', Q4N') corresponding to the logic complements of the remaining two local timing signals (Q2, Q4).

Add A27